# Logical Effort Designing Fast Cmos Circuits

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### Logical Effort Designing

**Logical Effort - Stanford University**
Logical Effort*: Designing for Speed on the Back of an Envelope David Harris harrisd@vlsistanfordedu August, 1998 Stanford University Stanford, CA * Based on a …
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Logical Effort*: Designing for Speed on the Back of an Envelope David Harris harrisd@vlsistanfordedu August, 1998 Stanford University Stanford, CA * Based on a …
**Logical Effort: Outline**
Logical Effort: Designing for Speed on the Back of an Envelope David Harris David_Harris@hmcedu Harvey Mudd College Claremont, CA Logical Effort David Harris Page 2 of 56 Outline Introduction Delay in a Logic Gate Multi-stage Logic Networks Choosing the Best Number of Stages Example
**Introduction to CMOS VLSI Design - UTEP**
Logical Effort CMOS VLSI Design Slide 13 Computing Logical Effort ! DEF: Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current ! Measure from delay vs fanout plots ! Or estimate by counting transistor widths A Y A B Y A B Y 1 2 1 1 2 2 2 2 4 4 C in = 3 g = 3/3
**Logical Effort: Designing Fast CMOS Circuits**
logical effort, suggesting that logical effort is a very natural way to think about de-lays He gradually discovered more properties of circuits, especially regarding the logical effort of other circuit families such as domino, and applied the principles of logical effort to …
**Lecture 6: Logical Effort**

6: Logical Effort CMOS VLSI DesignCMOS VLSI Design 4th Ed 4 Example Ben Bitdiddle is the memory designer for the Motoroil 68W86, an embedded automotive processor Help Ben design the decoder for a register file Decoder specifications: – 16 word register file – Each word is 32 bits wide – Each bit presents load of 3 unit-sized transistors

**Lecture 5: Logical Effort**

5: Logical Effort Slide 13CMOS VLSI Design Computing Logical Effort DEF: Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current Measure from delay vs fanout plots Or estimate by counting transistor widths AY A B Y A B Y 1 2 11 22 2 2 4 4 C in = 3 g = 3/3 C in

**Lecture 5: Logical Effort**

5: Logical Effort CMOS VLSI Design Slide 13 Computing Logical Effort qDEF: Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current qMeasure from delay vs fanout plots qOr estimate by counting transistor widths A Y A B Y A B Y 1 2 1 1 2 2 2 2 4 4 C in = 3 g = 3/3

**CMOS Design Optimization – Logical Effort**

1 EE141 – Fall 2005 Lecture 14 CMOS Design Optimization – Logical Effort EE141 2 Administrative Stuff PROJECT 1 (Start early!) • You will not be able to finish in 1 week! LABS • This week: Finish any remaining SW labs • Next week: Project help in labs HOMEWORKS • Due date for Hw6 = Mon Oct 24 (EE142 Midterm) • No new homework this week

**Chapter 4 Calculating the Logical Effort of Gates**

62 CHAPTER 4 CALCULATING THE LOGICAL EFFORT OF GATES where C b is the combined input capacitance of every signal in the input group b, and C inv is the input capacitance of an inverter designed to have the same drive

**The Method of Logical Effort**

The Method of Logical Effort 1 Designing a circuit to achieve the greatest speed or to meet a delay constraint presents a bewildering array of choices Which of several circuits that produce The method of logical effort is an easy way to estimate delay in a cmos circuit

**Designing for Speed on the Back of an Envelope David Harris**

Logical Effort David Harris Page 3 of 56 Introduction Chip designers face a bewildering array of choices o What is the best circuit topology for a function? o How large should the transistors be? o How many stages of logic give least delay? Logical Effort is a method of answering these questions:

**UT Austin, ECE Department VLSI Design 6. Logical Effort**

Logical Effort 15 Designing Fast Circuits • Delay is smallest when each stage bears same effort • Thus minimum delay of N stage path is • This is a key result of logical effort • Find fastest possible delay • Doesn’t require calculating gate sizes

**Download Logical Effort: Designing Fast CMOS Circuits ...**

Logical Effort: Designing Fast CMOS Circuits, Ivan Edward Sutherland, Robert F Sproull, David F Harris, Morgan Kaufmann, 1999, 1558605576, 9781558605572, 239 pages Designers of high-speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets

**Decoders: Logical Effort AppliedDecoders: Logical Effort ...**

We have now gone through the basics of decoders, and logical effort This lecture will use logical effort to optimize the perf f d d d i th ti tformance of

a decoder, and in the process motivate some ‘creative’ ways to build CMOS logic gates One result of this process will be a need to analyze slightly more complex

**CMPEN 411 VLSI Digital Circuits Spring 2012 Lecture 12 ...**

Sp12 CMPEN 411 L12 S5 First proposed by Ivan Sutherland and Bob Sproull in 1991 “Logical Effort: Designing for Speed on the back of an Envelope”, IEEE Advanced Research in VLSI, 1991 Both authors are vice president and fellow at Sun Microsystems Gain-based synthesis based on Logical effort Implemented in IBM’s logic synthesis tool BooleDozer

**CMPEN 411 VLSI Di it l Ci itVLSI Digital Circuits Spring ...**

CMPEN 411 VLSI Di it l Ci itVLSI Digital Circuits Spring 2011 Lecture 12: Logical Effort [Adapted from Rabaey’s Digital Integrated Circuits, Second Edition, ©2003 J Rabaey, A Chandrakasan, B Nikolic]

**CMOS Speed: Method of “Logical Effort”**

circuit They called it the method of “logical effort” The method brings the following important contributions to the art of circuit design: (a) Provides a quick way of estimating delay of a path (b) Provides a simple way of estimating optimal transistor sizes with the objective of …

**Unified Logical Effort- Delay Minimization Method in Logic ...**

these questions It is called Unified Logical Effort (ULE)[1] The Unified Logical Effort is an easy way of delay evaluation and minimization in CMOS circuits It is an extension of the Logical Effort model, which was first introduced by Sutherland [2],[3] This method considers only the delay caused by …

**Lecture 8: Logic Effort and Combinational Circuit Design**

Logical Effort CMOS VLSI Design 4th Ed 4 Computing Logical Effort q DEF: Logical effort is the ratio of the input capacitance of a gate to the input capacitance of an inverter delivering the same output current q Measure from delay vs fanout plots q Or estimate by counting transistor widths A Y A B Y A B Y 1 2 1 1 2 2 2 2 4 4 C in = 3 g = 3